FACULTY DEVELOPMENT PROGRAMME (FDP)

on

Low Power MOS Circuit Design and Testing

(10th to 15th June 2019)

Organized by

ELECTRONICS & ICT ACADEMY, NIT WARANGAL

at

Academic Staff College, KL University, Vaddeswaram, A.P.

(Sponsored by Ministry of Electronics and Information Technology (MEITY), GOI)

Preamble:

"Electronics & ICT Academy" was set up at NIT Warangal with financial assistance from MeitY, Govt. of India (GoI). The jurisdiction of this academy is Telangana, Andhra Pradesh, Andaman and Nicobar Islands, Goa, Puducherry and Karnataka states/UTs. This academy role is to offer faculty development programmes in standardized courses and emerging areas of Electronics, Information Communication Technologies, Curriculum development for Industry, Training & Consultancy services for Industry; CEP for working professionals, Advice and support for technical incubation and entrepreneurial activities.

Current trends demand for efficient and secured electronic systems for commercial and industrial applications. Internet of Things (IoT) is one of the major technology transcending industry, academia and government supporting the demands. It is projected that GDP due to IoT market is going to be $15 trillion which is larger than the GDP of India ($6.6 Trillion) by 2030. In this context, IoT became an essential component to make of our daily routine smart and secure. Considering the current thrust on Information Communication Technologies and Electronic Sector Design and Manufacturing by Government of India, and in view of the Internet of Things Policy of India, there is an immediate requirement for building capacity and expertise around Internet of Things.

Objectives of This FPD: In the current World, Very Large Scale Integration (VLSI) is considered to be one of the fastest growing cutting edge technologies. Each and every gadget which we use in day-to-day life involves VLSI directly or indirectly. With the development of Digital Signal Processors and High Performance Computing, VLSI based design has become the technology of choice. Requirement of miniaturization of the devices lead to more and more compact and efficient design structure. This Faculty Development Programme aims at introducing the participants to some of the recent technologies and refurbishes the VLSI MOS circuits with extensive hands on exposure.

Course Contents:

- Sources of Power Dissipation
- Low Power Digital and Analog MOS Circuits:
  - Reducing Glitches
  - Logic Level Power Optimization
  - Standby Mode Leakage Suppression
  - Variable Body Biasing
  - Sleep Transistors
  - Adiabatic Circuits
- Low-Power MOS Circuits Design Techniques:
  - System: Partitioning, Power down
  - Algorithm: Complexity, Concurrency, Regularity
  - Architecture: Parallelism, Pipelining, Redundancy, Data Encoding
  - Circuit Logic: Logic Styles, Energy Recovery, Transistor Sizing
  - Technology: Threshold Reduction, Multithreshold Devices
- Hands on session on the above topics will be provided

Faculty Conducting this Programme:

The programme will be conducted by the faculty members from NIT Warangal. Academicians from **IITs/ NITs /IIITs** in concerned field are invited to deliver lectures in the programme. Speakers from industries are also expecting to deliver lectures.

Eligibility:

The programme is open to the faculty of engineering colleges and other allied disciplines in India. Industry personnel working in the concerned/allied discipline can also attend.

Organized at:

The programme will be coordinated KL deemed to be University, Vaddeswaram, Guntur, A.P.

Accommodation:

All the outstation selected participants will be provided FREE boarding & lodging in university hostels. No TA will be paid for the participants.

Venue: C-Block, Sunflower Hall, KL University.

Registration Fee Particulars:

- **Faculty/Research Scholars : Rs. 2,500/- Only**
- **SC/ST Faculty : Rs.1,875/- Only**
  (Should submit Caste Certificate to claim concession)
- **Industry participants : Rs. 7,500/- Only**

SC/ST Concession is only for Faculty of mentioned states. Research scholars are not eligible for SC/ST Concession.

The participants need to send a crossed demand draft (DD) drawn in favor of "**Electronics & ICT Academy NITW, NIT Warangal**" and payable at SBI, NIT Warangal branch or remit the necessary course fee to the Bank as per the details given below.

Account Name	Electronics & ICT Academy NITW
Account Number	62423775910
Name	State Bank of India
Branch	REC Warangal (NIT Campus)
Branch Code	20149
IFSC	SBIN0020149

How to Apply:

A filled in form of application in the prescribed format duly signed and sponsored by appropriate authorities (along with DD/NEFT Receipt) should reach the coordinator by speed post. It is also mandatory to send scanned application form &DD/ NEFT receipt through e-mail to **fazalnoorbasha@kluniversity.in** as selection will be intimated only through mail.

Selection Criteria:

Selection will be done based on ***first-cum-first-serve basis*** and the confirmed candidates will be notified immediately. The maximum number of participants will be **50 (fifty)**. Additionally 10 participants from industry are allowed to participate. The list of selected participants will be sent to their personal *e-mail* ids. In case a candidate is not selected, the demand draft will be sent back. A test will be conducted at the end of the course. Candidates will be issued satisfactory certificate on successful completion of the course. Reservations are followed for selecting candidates as per **GOI** norms.

Important Dates:

Last date for submission of application : **1st June 2019**

Selection-list intimation/display before : **5th June 2019**

Duration of Program : **10th to 15th June 2019**

About NIT Warangal:

National Institute of Technology (formerly Regional Engineering College), Warangal is the first among 17 RECs setup as joint venture of the Government of India and the state government. Over the years the college has established itself as a premier Institution imparting technical education of a very high standard leading to the B.Tech degrees in various branches of engineering, M.Tech & Ph.D programs in various specializations. All B. Tech and M. Tech programmes of NIT Warangal are NBA accredited.

About KLU:

The Koneru Lakshmaiah Charities was established as a trust in the year 1980 and started K L College of Engineering in the Academic year 1980-81 and has attained autonomous status in the year 2006 and in February 2009, the Koneru Lakshmaiah Education Foundation Society was recognized as Deemed to be University and also the first to accredited with NAAC A++. It offers 23 UG programs, 26 PG programs, 28 integrated degree programs and dual degree programs. In addition to the research program in 14 disciplines, KLU has the credit of housing world class Centers of Excellence to boost research in emerging areas.

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APPLICATION FORM

1. Name of the Applicant:
2. Designation :
3. Institution :
4. E-mail ID :
5. Mobile No. :
6. Category
7. Payment Mode

☐ Faculty/Scholars	(Rs. 2,500/-)	☐ Demand Draft No: _____	
☐ SC/ST Faculty from mentioned states	(Rs. 1,875/-)	☐ NEFT/ UTR No. : _____	
☐ Industry Participants	(Rs. 7,500/-)	Bank: _____	Date : _____

8. Address for Correspondence:
9. Subjects taught so far:
10. Educational Qualifications with specialization:
11. No. of refresher courses/workshops attended:
12. Experience (in years) : ☐ Teaching ☐ Research ☐ Industry ☐
13. Do you belong to reservations SC/ST **(YES / NO)**:If YES, please specify **Attach photo copy
14. Do you require accommodation during Training : **YES /NO**

Declaration

The information provided is true to the best of my knowledge. If selected, I agree to abide by the rules and regulations of the FDP and shall attend the course for the entire duration. I also under take the responsibility to inform the Coordinator in case, I am unable to attend the course.

Place :
Date : **Signature of the Applicant**

SPONSORSHIP CERTIFICATE

Dr./Mr./Ms.……..……is an employee of our Institute/Organization and is here by sponsored to participate in the FDP on **"Low Power MOS Circuit Design and Testing"** sponsored by Electronics & ICT Academy during **10th to 15th June, 2019** at K L University.

Place :
Date : **Signature of Principal/Head of Institution**

Address for correspondence

Post your application form along with DD/NEFT Receipt to

Dr. Fazal Noorbasha
Associate Professor,
Dept. of ECE
K L University,
Vaddeswaram, AP - 522502.
Email: fazalnoorbasha@kluniversity.in
Mobile: 9000502785

Coordinators:

Dr. P Srihari Rao
Assoc. Prof,
Dept. of ECE,
NIT Warangal.
Telangana.

Dr. Fazal Noorbasha
Assoc. Prof,
Dept. of ECE
K L University
Andhra Pradesh

For more details about Electronics and ICT academy please visit: **http://www.nitw.ac.in/eict/**